Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of manufacturing a microelectronics device, comprising:

providing a substrate having an active layer, a dielectric layer and a structural layer, wherein the active layer is formed over the dielectric layer and the dielectric layer is formed over the structural layer;

forming an opening through the active layer thereby exposing a surface of the dielectric layer and defining active layer sidewalls; ~~and~~

forming a spacer covering a first portion of the exposed dielectric layer surface and substantially spanning one of the active layer sidewalls; and

forming a gate electrode over the active layer.

2. (Original) The method of claim 1 further comprising forming an etch stop layer over the active layer, wherein the opening is formed through the active layer and the etch stop layer thereby defining etch stop layer sidewalls substantially aligned with the active layer sidewalls, wherein the spacer substantially spans one of the active layer sidewalls and one of the etch stop layer sidewalls.

3. (Original) The method of claim 1 further comprising:

cleaning at least a second portion of the exposed dielectric layer surface.

4. (Original) The method of claim 3 wherein the cleaning includes chemical etching with an etchant chemistry comprising hydrofluoric acid.

5. (Original) The method of claim 3 wherein the cleaning includes plasma etching.

6. (Original) The method of claim 5 wherein the plasma etching includes a plasma chemistry comprising fluorine.

7. (Original) The method of claim 3 wherein the cleaning includes vapor etching.

8. (Cancelled).

9. (Original) The method of claim 1 further comprising forming a silicide layer over the active layer.

10. (Original) The method of claim 1 wherein the spacer comprises silicon dioxide.

11. (Original) The method of claim 1 wherein the active layer comprises strained silicon.

12. (Original) The method of claim 1 wherein the active layer has a thickness ranging between about 100 Angstroms and about 1000 Angstroms.

13-24. (Cancelled).

25. (New) A method of manufacturing a microelectronics device, comprising:

providing a substrate having:

a structural layer;

a dielectric layer located on the dielectric layer; and

an active layer located on the dielectric layer;

forming an opening through the active layer thereby exposing a surface of the dielectric layer and defining active layer sidewalls;

forming a spacer covering at least a portion of the exposed dielectric layer surface and spanning at least a portion of the active layer sidewalls; and

forming a gate electrode on the active layer.

26. (New) The method of claim 25 further comprising forming an etch stop layer over the active layer, wherein the opening is formed through the active layer and the etch stop layer thereby defining etch stop layer sidewalls substantially aligned with the active layer sidewalls, wherein the spacer substantially spans one of the active layer sidewalls and one of the etch stop layer sidewalls.

27. (New) The method of claim 25 further comprising:

cleaning at least a second portion of the exposed dielectric layer surface.

28. (New) The method of claim 27 wherein the cleaning includes chemical etching with an etchant chemistry comprising hydrofluoric acid.

29. (New) The method of claim 27 wherein the cleaning includes at least one of plasma etching and vapor etching.

30. (New) The method of claim 29 wherein the plasma etching includes a plasma chemistry comprising fluorine.

31. (New) The method of claim 25 further comprising forming a silicide layer over the active layer.

32. (New) The method of claim 25 wherein the spacer comprises silicon dioxide.

33. (New) The method of claim 25 wherein the active layer comprises strained silicon.

34. (New) The method of claim 25 wherein the active layer has a thickness ranging between about 100 Angstroms and about 1000 Angstroms.

35. (New) A method of manufacturing a microelectronics device on a substrate that includes a first dielectric layer located over a structural layer, the method comprising;

forming an active layer over a portion of the first dielectric layer;

forming spacers over the first dielectric layer and adjacent opposing ends of the active layer;

forming source/drain regions in the active layer, the source/drain regions extending laterally-inward from the opposing ends of the active layer; and

forming a second dielectric layer over at least a portion of the active layer.

36. (New) The method of claim 35 further comprising forming an etch stop layer over a substantial portion of the active layer prior to forming the spacers, wherein forming the spacers includes forming the spacers adjacent the opposing ends of the active layer and opposing ends of the etch stop layer such that the spacers span the active layer ends and at least portions of the etch stop layer ends.

37. (New) The method of clam 35 further comprising forming a gate electrode over at least a portion of the second dielectric layer.